

Appl. No. 10/707,968
Amdt dated November 21, 2006
Response to Office Action of August 21, 2006

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (currently amended) A method of fabricating a gate electrode for a semiconductor comprising the steps of:

providing a substrate prepared with a gate stack, the gate stack includes a gate dielectric on the substrate and a gate layer on the gate dielectric, the gate layer comprising, providing on the substrate a layer of a first material of thickness t_p , the first material being selected from the group consisting of Si, $Si_{1-x}Ge_x$ alloy, Ge and mixtures thereof,

providing and a metal layer on the gate layer, the metal layer having a metal of thickness t_m , and

annealing the layers, such that substantially all of the first material of the gate layer and metal of the metal layer over the gate layer are consumed during reaction with one another to form a resulting layer which serves as the gate electrode in contact with the gate dielectric.

2. (currently amended) The method of claim 1, wherein the metal layer comprises a metal is selected from one of the group consisting of Ni, Pd, Pt, Co, Ti and alloys of these materials including Ni-Pt, Ni-Pd, Ni-Co.

3. (currently amended) The method of claim 1, wherein the gate stack further comprises dielectric sidewall spacers and providing the first material layer is applied to the substrate and the metal layer comprises depositing the metal layer is provided on the first material layer.

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4. (original) The method of claim 1 wherein the thicknesses t_p and t_m are related by a predetermined ratio of t_m/t_p .
5. (original) The method of claim 4, wherein the ratio of t_m/t_p is determined by the particular first material and metal to be annealed.
6. (original) The method of claim 1 wherein annealing is performed at temperatures ranging from 300 to 900°C.
7. (original) The method of claim 1 further comprising the step of depositing a further layer of metal on the gate electrode to increase gate thickness.
8. (original) The method of claim 7 comprising forming source/drain contacts simultaneously with the gate electrode.
9. (original) The method of claim 8, wherein as much as 5% of one of the first material and the metal remains following reaction with the other of the metal and the first material.
10. (currently amended) A The gate electrode for a semiconductor device comprising:
a substrate with a gate stack formed thereon, the gate stack includes a gate dielectric on the substrate and the gate electrode on the gate dielectric,
wherein the gate electrode comprises a first material and a metal which have been substantially consumed and a gate layer thereon formed by the annealing of a first material with

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~~a metal, substantially all of the first material and the metal having been consumed during reaction with one another caused by annealing, the resultant layer comprising the gate electrode.~~

11. (original) The gate electrode of claim 10, wherein the metal is selected from one of the group consisting of Ni, Pd, Pt, Co, Ti and alloys of these materials including Ni-Pt, Ni-Pd, Ni-Co.

12. (original) The gate electrode of claim 10, wherein the first material is selected from the group consisting of Si, $Si_{1-x}Ge_x$ alloy, Ge and mixtures thereof.

13. (original) The gate electrode of claim 10 wherein as much as 5% of one of the first material and the metal remains following reaction with the other of the metal and the first material.

14. (currently amended) The gate electrode of claim 13, wherein a layer of metal is provided on the gate layer first material.

15. (original) The gate electrode of claim 10 wherein the gate electrode is incorporated in a CMOS semiconductor device.

16. (currently amended) A method for forming an integrated circuit comprising:
providing a substrate prepared with a first gate stack with dielectric sidewall spacers on the substrate and first and second diffusion regions in the substrate adjacent to the gate stack, the gate stack includes a gate dielectric on the substrate and a gate layer on the gate dielectric;

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depositing the gate layer comprises an amorphous or polycrystalline material first layer on the substrate, the first layer comprising a material having a work function close to the mid-gap of silicon band gap;

depositing a metal layer over the substrate covering the gate stack and diffusion regions; processing the metal layer to cause a reaction between the gate layer and the metal layer such that substantially all the material of the gate layer and portions of the metal layer over the gate layer are consumed to form a resulting layer which serves as the gate electrode which contacts the gate dielectric

patternning the first layer to form a gate electrode of a transistor and forming first and second diffusion regions of the transistor; and

wherein the material of the first layer reduces problems associated with inversion and agglomeration associated with formation of the transistor is reduced.

17. (currently amended) The method of claim 16 wherein:

the substrate is prepared with at least first and second gate stacks with dielectric sidewall spacers on the substrate and first and second diffusion regions in the substrate adjacent to the gate stacks, the gate stacks include a gate dielectric on the substrate and a gate layer on the gate dielectric, the first and second gate stacks serving as patterning the first layer comprises forming gate electrodes of at least a first PMOS transistor and a first NMOS transistor to form a CMOS integrated circuit; and

the material of the first gate layer comprises silicon, germanium, alloys or a combination thereof, including $\text{Si}_{1-x}\text{Ge}_x$.

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18. (currently amended) The method of claim 16 wherein the material of the gate first layer comprises silicon, germanium, alloys or a combination thereof, including $Si_{1-x}Ge_x$.
19. (currently amended) The method of claim 17 16 further comprises:
~~depositing a metal layer over the substrate after the gate electrode and diffusion regions of the transistor are formed; and~~
~~processing the metal layer to cause a reaction between the material of the first layer and metal layer such that substantially all the material of the first layer and portion of the metal layer over the first layer are consumed wherein a metal material of the metal layer is selected from one of the group consisting of Ni, Pd, Pt, Co, Ti and alloys of these materials including Ni-Pt, Ni-Pd, Ni-Co.~~
20. (currently amended) The method of claim 16 19 wherein processing the metal layer comprises annealing or rapid thermal annealing.
21. (currently amended) The method of claim 20 wherein unconsumed gate first layer is less than or equal to 5% and unreacted metal layer is less than or equal to 10%.
22. (currently amended) The method of claim 16 19 wherein the processing the metal layer also forms silicide over the diffusion regions.
23. (original) The method of claim 22 wherein processing the metal layer comprises annealing or rapid thermal annealing.

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24. (currently amended) The method of claim 23 wherein unconsumed first gate layer is less than or equal to 5% and unreacted metal layer is less than or equal to 10%.
25. (currently amended) The method of claim 16-19 wherein a metal material of the metal layer comprises Ni, Pd, Pt, Co, Ti, or a combination ~~or~~ of alloys thereof including Ni-Pt, Ni-Pd, and Ni-Co.
26. (currently amended) The method of claim 25 wherein the processing the metal layer also forms silicide over the diffusion regions.
27. (original) The method of claim 26 wherein processing the metal layer comprises annealing or rapid thermal annealing.
28. (original) The method of claim 25 wherein processing the metal layer comprises annealing or rapid thermal annealing.
29. (currently amended) The method of claim 16-19 wherein the first gate layer comprises a first thickness thickness t_p , and the metal layer comprises a second thickness t_m , and wherein a minimum of a ratio of the first and second thickness t_p/t_m results in consumption ~~or~~ of substantially the first gate and metal layers during processing of the metal layer.
30. (original) The method of claim 29 wherein processing the metal layer comprises annealing.

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31. (currently amended) The method of claim 29 wherein the processing the metal layer also forms silicide over the diffusion regions.
32. (original) The method of claim 31 wherein processing the metal layer comprises annealing or rapid thermal annealing.
33. (currently amended) The method of claim 16 ~~49~~ further comprises etching remaining portion of unreacted metal layer above the gate electrode after processing the metal layer.
34. (original) The method of claim 33 wherein processing the metal layer comprises annealing.
35. (currently amended) The method of claim 34 wherein the processing the metal layer also forms silicide over the diffusion regions.
36. (original) The method of claim 35 wherein processing the metal layer comprises annealing or rapid thermal annealing.
37. (currently amended) The method of claim 17 ~~49~~ wherein the first gate layer comprises a first thickness thickness t_p and the metal layer comprises a second thickness t_m , and wherein a minimum of a ratio of the first and second thickness t_p/t_m results in consumption ~~or of~~ substantially the first gate and metal layers during processing of the metal layer.

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38. (original) The method of claim 37 wherein processing the metal layer comprises annealing.

39. (currently amended) The method of claim 37 wherein the processing the metal layer also forms silicide over the diffusion regions.

40. (original) The method of claim 39 wherein processing the metal layer comprises annealing or rapid thermal annealing.

41. (currently amended) An integrated circuit comprising:
a transistor disposed on a substrate, the transistor having
a gate stack with a gate dielectric disposed on the substrate and a gate electrode
disposed on and in contact with the gate dielectric, and
first and second diffusion regions adjacent to the gate stack,
having a gate electrode and first and second diffusion regions wherein the gate electrode
is formed from an amorphous or polycrystalline first layer comprising a material and a metal
layer which have been substantially consumed during reaction with one another caused by
annealing having a work function close to the mid-gap of silicon band gap, wherein the material
reduces problems associated with inversion and agglomeration associated with formation of the
transistor is reduced.